2023 (MR23)

ENGINEERING (PG) CURRICULUM

M.Tech VLSI Regular

(Applicable for the batches admitted from 2023-24)

MALINENI LAKSHMAIAH WOMEN'S ENGINEERING COLLEGE

(AUTONOMOUS)

(Accredited by "NBA" & "NAAC" with A+ Grade | Approved by AICTE, New Delhi & Affiliated to JNTUK, Kakinada)

Pulladigunta(Vil), Vatticherukuru (Md), Prathipadu Road, Guntur - 522 017

Andhra Pradesh. www. mlewguntur.com

MALINENI LAKSHMAIAH WOMEN'S ENGINEERING COLLEGE

(AUTONOMOUS)

(Accredited by "NBA" & "NAAC" with A+ Grade | Approved by AICTE, New Delhi & Affiliated to JNTUK, Kakinada)

Pulladigunta(Vil), Vatticherukuru (Md), Prathipadu Road, Guntur - 522 017

Andhra Pradesh. www. mlewguntur.com

ACADEMIC REGULATIONS (MR23)

For

Master of Technology (M.Tech) Programme

(Duration: **Two Years)**

(Applicable for the batches admitted from A.Y. **2023-24**)

ACADEMIC REGULATIONS

Applicable for the students of M. Tech (Regular) Course from the Academic Year 2023-24 onwards. The M. Tech Degree shall be conferred on candidates who are admitted to the program and who fulfil all the requirements for the award of the Degree.

1.0 ELIGIBILITY FOR ADMISSIONS

Admission to the above program shall be made subject to eligibility, qualification and specialization as prescribed by the University from time to time.

Admissions shall be made on the basis of merit/rank obtained by the candidates at the qualifying Entrance Test conducted by the University or on the basis of any other order of merit as approved by the University, subject to reservations as laid down by the Govt. from time to time.

2.0 AWARD Of M. Tech DEGREE

2.1 A student shall be declared eligible for the award of the M. Tech Degree, if he pursues a course of study in not less than two and not more than four academic years.

2.2 **The student shall register for all 68 credits and secure all the 68 credits.**

2.3 The minimum instruction days in each semester are 90.

3.0 A. PROGRAMME OF STUDY

The following specializations are offered at present for the M. Tech Programme of study.

M.Tech

1. M.Tech- VLSI
2. M.Tech- Computer Science & Engineering (CSE)
3. M.Tech- CSE (Artificial Intelligence)

3.0 B. Departments offering M. Tech Programmes with specializations are noted below:

ECE	M.Tech- VLSI
CSE	M.Tech- Computer Science & Engineering (CSE)
	M.Tech- CSE (Artificial Intelligence)

4.0 ATTENDANCE

4.1 A student shall be eligible to write University examinations if he acquires a minimum of 75% of attendance in aggregate of all the subjects/courses, and with minimum 50% in each and every course including practicals.

4.2 Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester shall be granted by the College Academic Committee.

4.3 Shortage of Attendance **below** 65% in aggregate shall not be condoned and not eligible to write their end semester examination of that class.

4.4 Students whose shortage of attendance is not condoned in any semester are not eligible to write their end semester examination of that class.

4.5 A prescribed fee shall be payable towards condonation of shortage of attendance.

4.6 A student shall not be promoted to the next semester unless he satisfies the attendance requirement of the present semester, as applicable. They may seek re-admission into that semester when offered next. If any candidate fulfils the attendance requirement in the present semester, he shall not be eligible for re-admission into the same class.

5.0 EVALUATION

The performance of the candidate in each semester shall be evaluated subject-wise, with a maximum of 100 marks for theory and 100 marks for practical, on the basis of Internal Evaluation and End Semester Examination.

5.1 For the theory subjects 75 marks shall be awarded based on the performance in the End Semester Examination and 25 marks shall be awarded based on the Internal Evaluation. The internal evaluation shall be made based on the **average** of the marks secured in the two Mid Term-Examinations conducted-one in the middle of the Semester and the other immediately after the completion of instruction. Each midterm examination shall be conducted for a total duration of 120 minutes with 4 questions (without choice) each question for 10 marks, and it will be reduced to 25 marks. End semester examination is conducted for 75 marks for all FIVE (5) questions (one question from one unit) to be answered (either or).

5.2 For practical subjects, 75 marks shall be awarded based on the performance in the End Semester Examinations and 25 marks shall be awarded based on the day-to-day performance as Internal Marks. The internal evaluation based on the

day to day work-5 marks, record- 5 marks and the remaining 15 marks to be awarded by conducting an internal laboratory test. The end examination shall be conducted by the examiners, with breakup marks of Procedure-20, Experimentation-30, Results-10, Viva-voce-15.

5.3 For Mini Project with Seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Project Review Committee consisting of Head of the Department, supervisor/mentor and two other senior faculty members of the department. For Mini Project with Seminar, there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

5.4 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Semester Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

5.5 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 5.4) he has to re-appear for the End Semester Examination in that subject. A candidate shall be given **one** chance to re-register for each subject provided the internal marks secured by a candidate **are less than 50% and has failed in the end examination.** In such a case, the candidate must re-register for the subject(s) and secure the required minimum attendance. The candidate's attendance in the re-registered subject(s) shall be calculated separately to decide upon his eligibility for writing the end examination in those subject(s). In the event of the student taking another chance, his internal marks and end examination marks obtained in the previous attempt shall stands cancelled. For re-registration the candidates have to apply to the University through the college by paying the requisite fees and get approval from the University before the start of the semester in which re-registration is required.

5.6 In case the candidate secures less than the required attendance in any re-registered subject(s), he shall not be permitted to write the End Examination in that subject. He shall again re-register the subject when next offered.

5.7 Laboratory examination for M. Tech. courses must be conducted with two Examiners, one of them being the Laboratory Class Teacher or teacher of the respective college and the second examiner shall be appointed by the University from the panel of examiners submitted by the respective college.

6.0 EVALUATION OF PROJECT/DISSERTATION WORK

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

6.1 A Project Review Committee (PRC) shall be constituted with Head of the Department and two other senior faculty members in the department.

6.2 Registration of Dissertation/Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects, both theory and practical.

6.3 After satisfying 6.2, a candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work for approval. The student can initiate the Project work, only after obtaining the approval from the Project Review Committee (PRC).

6.4 If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the Project Review Committee (PRC). However, the PRC shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

6.5 Continuous assessment of Dissertation-I and Dissertation-II during the Semester(s) will be monitored by the PRC.

6.6 A candidate shall submit his status report in two stages to the PRC, at least with a gap of 3 months between them.

6.7 The work on the project shall be initiated at the beginning of the II year and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis only after successful completion of theory and practical course with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. The candidate has to pass all the theory and practical subjects before submission of the Thesis.

6.8 Three copies of the Project Thesis certified by the supervisor shall be submitted to the College/School/Institute.

6.9 The thesis shall be adjudicated by one examiner selected by the University. For this, the Principal of the College shall submit a panel of 5 examiners, eminent in that field, with the help of the guide concerned and head of the department.

6.10 If the report of the examiner is not favourable, the candidate shall revise and resubmit the Thesis, in the time frame as decided by the PRC. If the report of the examiner is unfavorable again, the thesis shall be summarily rejected. The

candidate has to reregister for the project and complete the project within the stipulated time after taking the approval from the University.

6.11 The Head of the Department shall coordinate and make arrangements for the conduct of Viva-Voce examination.

6.12 If the report of the examiner is favourable, Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the examiner who adjudicated the Thesis. The Board shall jointly report the candidate's work for a maximum of 100 marks as one of the following:

A. Excellent

B. Good

C. Satisfactory

D. Unsatisfactory

6.13 If the report of the Viva-Voce is unsatisfactory (ie, < 50 marks), the candidate shall retake the Viva-Voce examination only after three months. If he fails to get a satisfactory report at the second Viva-Voce examination, the candidate has to re-register for the project and complete the project within the stipulated time after taking the approval from the University.

7.0 Cumulative Grade Point Average (CGPA)

Marks Range Theory/ Laboratory (Max – 100)	Marks Range Mini Project/ Project Work or Dissertation (Max – 100)	Letter Grade	Level	Grade Point
≥ 90	≥ 90	O	Outstanding	10
≥80 to <90	≥80 to <90	S	Excellent	9
≥70 to <80	≥70 to <80	A	Very Good	8
≥60 to <70	≥60 to <70	B	Good	7
≥50 to <60	≥50 to <60	C	Fair	6
≥40 to <50	≥40 to <50	D	Satisfactory	5
<40	<40	F	Fail	0
-	-	AB	Absent	0

Computation of SGPA

The following procedure is to be adopted to compute the Semester Grade Point Average (SGPA) and Cumulative Grade Point Average (CGPA):

The **SGPA** is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses undergone by a student, i.e

$$S = \frac{\sum_{i=1}^{n}(C_i \times G_i)}{\sum_{i=1}^{n} C_i}$$

where C_i is the number of credits of the i^{th} course and G_i is the grade point scored by the student in the i^{th} course and *'n'* is the number of courses/subjects registered in that semester.

Computation of CGPA

The **CGPA** is also calculated in the same manner taking into account all the *'m'* courses/subjects undergone by a student over all the semester of a Programme, i.e.

$$C = \frac{\sum_{i=1}^{m}(C_i \times S_i)}{\sum_{i=1}^{m} C_i}$$

where S_i is the SGPA of the i^{th} semester and C_i is the total number of credits in that semester.

The SGPA and CGPA shall be rounded off to 2 decimal points and reported in the transcripts.

Equivalent Percentage = (CGPA – 0.75) x 10

8.0 AWARD OF DEGREE AND CLASS

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree he shall be placed in one of the following four classes:

Class Awarded	**CGPA to be secured**	
First Class with Distinction	≥ 7.75	**From the CGPA Secured from 68 Credits.**
First Class	≥ 6.75 and < 7.75	
Second Class	≥ 5.75 to < 6.75	
Pass Class	≥ 4.75 to < 5.75	

The Grades secured, Grade points and Credits obtained will be shown separately in the memorandum of marks.

9.0 WITHHOLDING OF RESULTS

If the student is involved in indiscipline/malpractices/court cases, the result of the student will be withheld.

10.0 TRANSITORY REGULATIONS

10.1 Discontinued or detained candidates are eligible for re-admission into same or equivalent subjects at a time as and when offered.

10.2 The candidate who fails in any subject will be given two chances to pass the same subject.

11.0 GENERAL

11.1 Wherever the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”, “hers”.

11.2 The academic regulation should be read as a whole for the purpose of any interpretation.

11.3 In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Principal is final.

11.4 The Institute may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the College.

MALPRACTICES RULES

DISCIPLINARY ACTION FOR / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/Improper	**conduct**
	If the candidate:	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In

	communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the University.
3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate, who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate

	answer book or additional sheet, during or after the examination.	has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
6.	Refuses to obey the orders of the Chief Superintendent/Assistant – Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officerin-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.

	disrupt the orderly conduct of the examination.	
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be

		registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action to award suitable punishment.	

Malpractices identified by squad or special invigilators

1. Punishments to the candidates as per the above guidelines.
2. Punishment for institutions: (if the squad reports that the college is also involved in encouraging malpractices)
   (i) A show cause notice shall be issued to the college.
   (ii) Impose a suitable fine on the college.
   (iii) Shifting the examination centre from the college to another college for a specific period of not less than one year.

MALINENI LAKSHMAIAH WOMEN'S ENGINEERING COLLEGE

(AUTONOMOUS)

(Accredited by "NBA" & "NAAC" with A+ Grade | Approved by AICTE, New Delhi & Affiliated to JNTUK, Kakinada)

Pulladigunta(Vil), Vatticherukuru (Md), Prathipadu Road, Guntur - 522 017

Andhra Pradesh. www. mlewguntur.com

COURSE STRUCTURE & SYLLABUS

MASTER OF TECHNOLOGY

in

VERY LARGE SCALE INTEGRATION (VLSI)

(FOR **Two-Year PG Programme)**

(Applicable for batches admitted from 2023-24)

SEMESTER-WISE COURSE STRUCTURE

Semester-I **M.Tech. (VLSI)**

S.No	Course Code	Course Name	L	T	P	Credits
1	23MTVLT01	CMOS Analog IC Design	3	0	0	3
2	23MTVLT02	CMOS Digital IC design	3	0	0	3
3	23MTVLE01 23MTVLE02 23MTVLE03	**Professional Elective 1:** 1. VLSI Technology 2. Nanomaterials and Nanotechnology 3. MEMS Technology	3	0	0	3
4	23MTVLE04 23MTVLE05 23MTVLE06	**Professional Elective 2:** 1. Device Modeling 2. Nano-electronics 3. Photonics	3	0	0	3
5	23MTVLT03	Research methodology and IPR	2	0	0	2
6	23MTVLL01	CMOS Analog IC Design Lab	0	0	4	2
7	23MTVLL02	CMOS Digital IC Design Lab	0	0	4	2
8	23MTVLAD7	Audit course-1	2	0	0	0
			Total			**18**

Semester-II **M.Tech. (VLSI)**

S.No	Course Code	Course Name	L	T	P	Credits
1	23MTVLT04	Mixed Signal & RF IC Design	3	0	0	3
2	23MTVLT05	Physical Design Automation	3	0	0	3
3	23MTVLE07 23MTVLE08 23MTVLE09	**Professional Elective 3:** 1. Design For Testability 2. IOT & its Applications 3. VLSI Signal Processing	3	0	0	3
4	23MTVLE10 23MTVLE11 23MTVLE12	**Professional Elective 4:** 1. Network Security & Cryptography 2. Microcontrollers & programmable Digital Signal Processors 3. Low Power VLSI Design	3	0	0	3
5	23MTVLL04	Mixed Signal IC Design Lab	0	0	4	2
6	23MTVLL05	Physical Design Automation Lab	0	0	4	2
7	23MTVLP01	Mini Project	0	0	4	2
8	23MTVLAD8	Audit Course – 2	2	0	0	0
			Total			**18**

* Students be encouraged to go to Industrial Training/Internship for at least 2-3 weeks during semester break.

Semester-III **M.Tech. (VLSI)**

S.No	Course Code	Course Name	L	T	P	Credits
1	23MTVLE13 23MTVLE14 23MTVLE15	**Professional Elective 5:** 1.Scripting Languages for VLSI 2. Digital System Design & Verification 3.Hardware Software co-design	3	0	0	3
2	23MTVLOE1 23MTVLOE2 23MTVLOE3 23MTVLOE4 23MTVLOE5 23MTVLOE6	**Open Elective:** 1. Business Analytics 2. Industrial Safety 3. Operations Research 4. Cost Management of Engineering Projects 5. Composite Materials 6. Waste to Energy	3	0	0	3
3	23MTVLP02	Dissertation Phase -I /Industrial Project **(to be continued and evaluated next semester)**	0	0	20	10#
			Total			**16**

#Evaluated and Displayed in IV Semester Marks list.

*Students going for Industrial Project/Thesis will complete these courses through MOOCs

Semester-IV **M.Tech. (VLSI)**

S.No	Course Code	Course Name	L	T	P	Credits
1	23MTVLP02	Project/ Dissertation Phase-II **(continued from III semester)**	0	0	32	16
			Total			**16**

Audit Course 1& 2

1. English for Research Paper Writing
2. Disaster Management
3. Sanskrit for Technical Knowledge
4. Value Education
5. Constitution of India
6. Pedagogy Studies
7. Stress Management by Yoga
8. Personality Development through Life Enlightenment Skills

CMOS ANALOG IC DESIGN (23MTVLT01)

Course Category	**PC**	Credits	**3**
Course Type	**Theory**	L-T-P	**3-0-0**
Year	**I**	CIE Marks	**25**
Sem.	**I**	SEE Marks	**75**
		Total Marks	**100**

Course Objectives:

- This course focuses on theory, analysis and design of analog integrated circuits in both Bipolar and Metal-Oxide-Silicon (MOS) technologies.
- Basic design concepts, issues and tradeoffs involved in analog IC design are explored.
- Intuitive understanding and real-life application sareemphasized throughout the course.
- To learn about Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascade Op Amps, Measurement Techniques of OP Amp.
- To know about Characterization of Comparator, Two-Stage, Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators etc.

Course Outcomes:

At the end of course, the student will be able to

Number	**COURSE OUTCOMES (COs)**	**Blooms Taxonomy**
CO1	Design MOSFET based analog integrated circuits	**L3**
CO2	Analyze analog circuits at least to the first order.	**L4**
CO3	Appreciate the trade-offs involved in analog in targeted circuit design.	**L3**
CO4	Understand and appreciate the importance of noise and distortion in analog circuits.	**L2**
CO5	Analyzecomplexengineeringproblemscriticallyinthedomainofanalog ICdesignforconductingresearch.	**L4**
CO6	Solve engineering problems for feasible and optimal solutions in the core area of analog ICs.	**L5**

***Note**: L1- Remember, L2 – Understand, L3 – Apply, L4 – Analyze, L5 – Evaluate, L6 – Create*

COURSE CONTENTS

UNIT-I

Basic MOS Device Physics – General Considerations, MOS I/V Characteristics, Second Order effects, MOS Device models. Short Channel Effects and Device Models. Single Stage Amplifiers–Basic Concepts, Common Source Stage, Source Follower, Common Gate Stage, Cas code Stage.

UNIT-II

Differential Amplifiers–Single Ended and Differential Operation, Basic Differential Pair, Common Mode Response, Differential Pair with MOS loads, Gilbert Cell. Passive and Active Current Mirrors– Basic Current Mirrors, Cas code Current Mirrors, Active Current Mirrors.

UNIT-III

Frequency Response of Amplifiers– General Considerations, Common Source Stage, Source Followers, Common Gate Stage, Cas code Stage, Differential Pair. Noise – Types of Noise, Representation of Noise in circuits, Noise in single stage amplifiers, Noise in Differential Pairs.

UNIT-IV

Feedback Amplifiers–General Considerations, Feedback Topologies, Effect of Loading. Operational Amplifiers– General Considerations, One Stage Op Amps, Two Stage Op Amps, Gain Boosting, Common–Mode Feedback, Input Range limitations, Slew Rate, Power Supply Rejection, Noise in Op Amps. Stability and Frequency Compensation.

UNIT-V:

Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

Text Books:

1. B. Razavi, "Design of Analog CMOS Integrated Circuits", 2nd Edition, McGrawHill Edition 2016.
2. Paul. R. Gray & Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley, 5th Edition, 2009.

Reference Books:

1. T.C. Carusone, D.A. Johns & K. Martin, "Analog Integrated Circuit Design", 2nd Edition, Wiley, 2012.
2. P.E. Allen & D.R. Holberg, "CMOS Analog Circuit Design", 3rdEdition, Oxford University Press, 2011.
3. R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", 3rdEdition, Wiley, 2010.
4. Recent literature in Analog IC Design.

CMOS DIGITAL IC DESIGN (23MTVLT02)

Course Category	**PC**	Credits	**3**
Course Type	**Theory**	L-T-P	**3-0-0**
Year	**I**	CIE Marks	**25**
Sem.	**I**	SEE Marks	**75**
		Total Marks	**100**

Course Objectives:

- To understand the fundamental properties of digital Integrated circuits using basic MOSFET equations and to develop skills for various logic circuits using CMOS related design styles.
- The course also involves analysis of performance metrics.
- To teach fundamentals of CMOS Digital integrated circuit design such as importance of Pseudo logic, Combinational MOS logic circuits, and Sequential MOS logic circuits.
- To teach the fundamentals of Dynamic logic circuits and basic semi conductor
- Memories which are the basics for the design no high performance digital integrated circuits.

Course Outcomes:

At the end of course, the student will be able to

Number	COURSE OUTCOMES (COs)	Blooms Taxonomy
CO1	Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS, Alternative CMOS Logics, Estimation of Delay and Power, Adders Design.	**L3**
CO2	Classify different semi conductor memories.	**L3**
CO3	Analyze, design and implement combinational and sequential MOS logic circuits.	**L4**
CO4	Analyze complex engineering problems critically in the domain of digital IC design for conducting research.	**L4**
CO5	Solveengineeringproblemsforfeasibleandoptimalsolutionsinthecor eareaofdigitalICs.	**L5**

***Note**: L1- Remember, L2 – Understand, L3 – Apply, L4 – Analyze, L5 – Evaluate, L6 – Create*

COURSE CONTENTS

UNIT-I: MOS Design

Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain atgatethres hold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT-II: Combinational MOS Logic Circuits:

MOS logic circuits with NMOS loads, Primitive CMOS logic gates–NOR& NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OAI gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT-III: Sequential MOS Logic Circuits

Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS Dlatchand edge triggered flip-flop.

UNIT-IV: Dynamic Logic Circuits

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT-V: Semiconductor Memories

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

Text Books:

1. Digital Integrated Circuit Design–Ken Martin, Oxford University Press,2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rdEd., 2011.

Reference Books:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective–Ming-BOLin, CRCPress, 2011
2. Digital Integrated Circuits–A Design Perspective, Jan M.Rabaey, Anantha Chandrakasan Borivoje Nikolic, 2nd Ed., PHI.

VLSI TECHNOLOGY (23MTVLE01)

Course Category	**PE/ELECTIVE-1**	Credits	**3**
Course Type	**Theory**	L-T-P	**3-0-0**
Year	**I**	CIE Marks	**25**
Sem.	**I**	SEE Marks	**75**
		Total Marks	**100**

Course Outcomes:

At the end of course, the student will be able to

Number	COURSE OUTCOMES (COs)	Blooms Taxonomy
CO1	Understand the basics of MOS transistors and also the characteristics of MOS transistors.	**L2**
CO2	Learn about the MOS fabrication process and short channel effects.	**L3**
CO3	Learn about the basic rules in layout designing.	**L3**
CO4	Analyze various combinational logic networks and sequential systems.	**L4**

***Note**: L1- Remember, L2 – Understand, L3 – Apply, L4 – Analyze, L5 – Evaluate, L6 – Create*

COURSE CONTENTS

UNIT-1: MOS Transistors

Introduction, The Structure of MOS Transistors, The Fluid Model, The MOS Capacitor, The MOS Transistor, Modes of Operation of MOS Transistors, Electrical Characteristics of MOS Transistors, Threshold Voltage, Transistor Trans conductance g_m, Figure of Merit, Body Effect, Channel-Length Modulation, MOS Transistors as a Switch, Transmission Gate

UNIT-2: MOS Fabrication Technology

Introduction, Basic Fabrication Processes, Wafer Fabrication, Oxidation, Mask Generation, Photolithography, Diffusion, Deposition. N-MOS Fabrication Steps, CMOS Fabrication Steps, n-Well Process, p-Well Process, Twin-Tub Process, Latch-Up Problem and Its Prevention, Use of Guard Rings, Use of Trenches, Short-Channel Effects-Channel Length Modulation Effect. Drain-Induced Barrier Lowering, Channel Punch Through, Hot carrier effect, Velocity Saturation Effect

UNIT-3: Layout Design Rules

Scaling Theory, Scalable CMOS Design Rules, CMOS Process Enhancements, Transistors, Interconnects, Circuit Elements, Efficient layout Design techniques

UNIT-4: Combinational Logic Networks

Layouts for logic networks. Delay through networks. Power optimization. Switch logic networks. Combination al logic testing

UNIT-5: Sequential Systems

Memory cells and Arrays, clocking disciplines, sequential circuit Design, Performance Analysis, Power optimization, Design validation and testing.

Text Books:

1. Principals of CMOS VLSI Design-N.H.E Weste, K.Eshraghian, 2nd Edition, Addison Wesley.
2. CMOS Digital Integrated Circuits Analysis and Design–Sung-MoKang, Yusuf Leblebici, TMH, 3rd Ed., 2011.
3. Low-Power VLSI Circuits and Systems, AjitPal, SPRINGER PUBLISHERS
4. Modern VLSI Design–Wayne Wolf, 3rdEd., 1997, Pearson Education.

Reference Books:

1. Digital Integrated Circuit Design –Ken Martin,Oxford University Press, 2011.
2. Digital Integrated Circuits –A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

NANOMATERIALS AND NANOTECHNOLOGY (23MTVLE02)

Course Category	**PE/ELECTIVE-1**	Credits	**3**
Course Type	**Theory**	L-T-P	**3-0-0**
Year	**I**	CIE Marks	**25**
Sem.	**I**	SEE Marks	**75**
		Total Marks	**100**

Course Outcomes:

At the end of course, the student will be able to

Number	COURSE OUTCOMES (COs)	Blooms Taxonomy
CO1	To understand the basic science behind the design and fabrication of nano scale systems.	**L2**
CO2	To understand and formulate new engineering solutions for current problems and competing technologies for future applications.	**L2**
CO3	To be able make interdisciplinary projects applicable to wide areas by clearing and fixing the boundaries in system development.	**L3**
CO4	To gather detailed knowledge of the operation of fabrication and characterization devices to achieve precisely designed systems.	**L4**

***Note**: L1- Remember, L2 – Understand, L3 – Apply, L4 – Analyze, L5 – Evaluate, L6 – Create*

COURSE CONTENTS

UNIT-I

Introduction of nano materials and nanotechnologies, Features of nanostructures, Applications of nano materials and technologies. Nano dimensional Materials 0D, 1D, 2D structures – Size Effects –Fraction of Surface Atoms –Specific Surface Energy and Surface Stress – Effect on the Lattice Parameter–Phonon Density of States–the General Methods available for the Synthesis of Nanostructures – precipitate – reactive– hydrothermal/solve thermal methods – suitability of such methods for scaling– potential Uses.

UNIT-II

Fundamentals of nano materials, Classification, Zero-dimensional nano materials, One-dimensional nano materials, Two-dimensional nano materials, Three dimensional nano materials. Low-Dimensional Nano materials and its Applications, Synthesis, Properties, and Applications of Low - Dimensional Carbon-Related Nano materials.

UNIT-III

Micro-and Nanolithography Techniques, Emerging Applications Introduction to Micro electro mechanical Systems (MEMS), Advantages and Challenges of MEMS, Fabrication Technologies, Surface Micro machining, Bulk Micromachining, Molding. Introduction to Nano Phonics.

UNIT-IV

Introduction, Synthesis of CNTs-Arc-discharge, Laser-ablation, Catalytic growth, Growth mechanisms of CNT‟s - Multi-walled nano tubes, Single-walled nano tubes Optical properties of CNT‟s, Electrical transportation perfect nano tubes, Application sascase studies. Synthesis and Applications of CNT's.

UNIT-V

Ferroelectric materials, coating, molecular electronics and nano electronics, biological and environmental, membrane based application, polymer based application.

Text Books:

1. Kenneth J. Klabunde and Ryan M. Richards, “Nano scale Materials in Chemistry”, 2nd edition, John Wiley and Sons, 2009.
2. I Gusev and AARempel, “Nano crystal in eMaterials”, Cambridge International Science Publishing, 1st Indian edition by Viva Books Pvt. Ltd. 2008.
3. B.S. Murty, P. Shankar, Baldev Raj, B. B. Rath, James Murday, “Nano science and Nano technology”, Tata McGraw Hill Education 2012.

Reference Books:

1. Bharat Bhushan, “Springer Handbook of Nano technology”, Springer, 3rdedition, 2010.
2. Kamal K.Kar, “Carbon Nano tubes: Synthesis, Characterization and Applications”, Research Publishing Services; 1st edition, 2011,ISBN-13:978-9810863975.

MEMS TECHNOLOGY (23MTVLE03)

Course Category	**PE/ELECTIVE-1**	Credits	**3**
Course Type	**Theory**	L-T-P	**3-0-0**
Year	**I**	CIE Marks	**25**
Sem.	**I**	SEE Marks	**75**
		Total Marks	**100**

Course Outcomes:

At the end of course, the student will be able to

Number	COURSE OUTCOMES (COs)	Blooms Taxonomy
CO1	To understand the basic concepts of MEMS technology and working of MEMS devices.	**L2**
CO2	To understand and selecting different materials for current MEMS devices and competing Technologies for future applications.	**L2**
CO3	To understanding the concepts of fabrication process of MEMS, Design and Packaging Methodology.	**L2**
CO4	To analyze the various fabrication techniques in the manufacturing of MEMS Devices.	**L4**

***Note**: L1- Remember, L2 – Understand, L3 – Apply, L4 – Analyze, L5 – Evaluate, L6 – Create*

COURSE CONTENTS

UNIT-I: Introduction to MEMS

Introduction to MEMS & Real world Sensor/Actuator examples (DMD, Air-bag, pressure sensors). MEMS Sensors in Internet of Things (IoT),Bio-Medical Applications

UNIT-II: MEMS Materials and Their Properties

Materials (eg. Si, SiO2, SiN, Cr, Au, Ti, SU8, PMMA, Pt); Important properties: Young modulus, Poisson "sratio, density, piezo-resistive coefficients, TCR, Thermal Conductivity, Material Structure. Understanding Selection of materials based on applications.

UNIT-III: MEMS Fab Processes–1

Understanding MEMS Processes & Process parameters for: Cleaning, Growth & Deposition, Ion Implantation & Diffusion, Annealing, Lithography. Understanding selection of Fab processes based on Applications.

UNIT-IV: MEMS Fab Processes–2

Understanding MEMS Processes & Process parameters for: Wet & Dry etching, Bulk& Surface Micro machining, Die, Wire & Wafer Bonding, Dicing, Packaging. Understanding selection of Fab processes based on Applications

UNIT-V: MEMS Devices

Architecture, working and basic quantitative behavior of Cantilevers, Micro heaters, Accelerometers, Pressure Sensors, Micro mirrors in DMD, Inkjet printer-head. Understanding steps involved in Fabricating above devices

Text Books:

1. An Introduction to Micro electromechanical Systems Engineering; 2ndEd-by N. Maluf, K Williams; Publisher: Artech HouseInc
2. Practical MEMS –by Ville Kaajakari; Publisher: Small Gear Publishing
3. Micro system Design-by S. Senturia; Publisher: Springer.

Reference Books:

1. Analysis and Design Principles of MEMS Devices-Minhang Bao; Publisher: Elsevier Science.
2. Fundamentals of Micro fabrication –by M. Madou; Publisher: CRC Press; 2nd edition.
3. Micro Electro Mechanical System Design-by J. Allen; Publisher: CRC Press.
4. Micro machined Transducers Sourcebook –by G. Kovacs; Publisher: McGraw-Hill.

DEVICE MODELING (23MTVLE04)

Course Category	**PE/ELECTIVE-II**	Credits	**3**
Course Type	**Theory**	L-T-P	**3-0-0**
Year	**I**	CIE Marks	**25**
Sem.	**I**	SEE Marks	**75**
		Total Marks	**100**

Course Outcomes:

At the end of course, the student will be able to

Number	COURSE OUTCOMES (COs)	Blooms Taxonomy
CO1	To understand the physics of 2-terminal MOS operation and its characteristics	**L2**
CO2	To understand the physics of 4-terminal MOSFET operation and its characteristics	**L2**
CO3	To analyze the SOIMOSFET electrical characteristics	**L4**

***Note**: L1- Remember, L2 – Understand, L3 – Apply, L4 – Analyze, L5 – Evaluate, L6 – Create*

COURSE CONTENTS

UNIT-I

2-terminal MOS device: threshold voltage modeling (ideal case as well as considering the effects of Qf, Φms and Dit.).

UNIT-II

C-V characteristics (ideal case as well as taking into account the effects of Qf, Φms and Dit); MOS capacitor as a diagnostic tool (measurement of non-uniform doping profile, estimation of Qf, Φms and Dit)

UNIT-III

4-terminal MOSFET: threshold voltage (considering the substratebias) ; above threshold I- V modeling(SPICE level1,2,3 and 4).

UNIT-IV

Sub threshold current model; scaling; effect of threshold tailoring implant (analytical modeling of threshold voltage using box approximation); buried channel MOSFET. Short channel, DIBL and narrow width effects; small signal analysis of MOSFETs (Meyer ‟smodel)

UNIT-V

SOIMOSFET: basic structure; threshold voltage modeling Advanced topics: hot carriers in channel; EEPROMs; CCDs; high-K gate dielectrics.

Text Books:

1. D.G. Ong, “Modern MOS Technology: Processes, Devices and Design”, McGraw Hill, 1984.
2. Y. Taurand T.H. Ning, “Fundamentals of modern VLSI Devices” Cambridge Univ. Press, 1998.
3. S.M. Sze, “Physics of Semiconductor Devices” Wiley, 1981.

NANO-ELECTRONICS (23MTVLE05)

Course Category	**PE/ELECTIVE-II**	Credits	**3**
Course Type	**Theory**	L-T-P	**3-0-0**
Year	**I**	CIE Marks	**25**
Sem.	**I**	SEE Marks	**75**
		Total Marks	**100**

Course Outcomes:

At the end of course, the student will be able to

Number	COURSE OUTCOMES (COs)	Blooms Taxonomy
CO1	To understand and challenges due to scaling on CMOS devices.	**L2**
CO2	To analyze and explain working of novel MOS based silicon devices and various multi gate devices.	**L4**
CO3	To understand working of spin electronic devices.	**L3**
CO4	To understand nano electronic systems and building blocks such as: low dimensional semiconductors, hetero structures, carbon nano tubes, quantum dots, nano wires etc.	**L3**

***Note**: L1- Remember, L2 – Understand, L3 – Apply, L4 – Analyze, L5 – Evaluate, L6 – Create*

COURSE CONTENTS

UNIT I

Properties of Individual Nano particles : Introduction, Metal Nano Clusters, Semi conducting Nano particles, Rare Gas and Molecular Clusters, Methods of Synthesis.

UNIT II

The nano scale MOSFET, Fin FETs, Vertical MOSFETs, limits to scaling, system integration limits (interconnect issues etc.),Resonant Tunnelling Transistors.

Carbon Nano Structures: Introduction, Carbon Molecules, Carbon Clusters, Carbon Nano Tubes, Application of Carbon Nanotubes.

UNIT III

Carbon Nano tubes for Data Processing – Introduction, Electronic Properties, Synthesis of Carbon Nano tubes, Carbon Nano tube Interconnects, Carbon Nano tubes Field Effect Transistors (CNTFETs), Nano tubes for Memory Applications, Prospects of an All-CNT Nano electronics. Neuro electronic Interfacing: Semi conductor Chips with Ion Channels, Nerve Cells, and Brain: Introduction, Iono-Electronic Inter face, Neuron-Silicon Circuits, Brain-Silicon Chips.

UNIT IV

Optical 3-D Time-of-Flight Imaging System: Introduction, Taxonomy of Optical 3-D Techniques, CMOS Imaging, CMOS 3-DTime-of-FlightImageSensor, Application Examples Pyroelectric Detector Arrays for IR Imaging: Introduction, Operation Principle of Pyroelectric IR Detectors, Pyroelectric Materials, Realized Devices, Characterization, and Processing Issues

UNIT V

Electronic Noses: Introduction, Operating Principles of Gas Sensor Elements, Electronic Noses, Signal Evaluation, Dedicated Examples.2-DTactileSensors and Tactile Sensor Arrays: Introduction, Definitions and Classifications, Resistive Touch screens, Ultrasonic Touch screens, Robot Tactile Sensors, Fingerprint Sensors

Text Books:

1. Introduction to Nanotechnology, C.P. PooleJr., F.J. Owens, Wiley (2003),
2. Nanoelectronics and Information Technology (Advanced Electronic Materials and Novel Devices), Waser Ranier, Wiley-VCH, 2003

Reference Books:

1. Nano systems, K.E. Drexler, Wiley (1992).
2. The Physics of Low-Dimensional Semiconductors, John H. Davies, “Cambridge University Press,"1998.

PHOTONICS (23MTVLE06)

Course Category	**PE/ELECTIVE-II**	Credits	**3**
Course Type	**Theory**	L-T-P	**3-0-0**
Year	**I**	CIE Marks	**25**
Sem.	**I**	SEE Marks	**75**
		Total Marks	**100**

Course Outcomes:

At the end of course, the student will be able to

Number	COURSE OUTCOMES (COs)	Blooms Taxonomy
CO1	Classify the Optical sources and detectors and to discuss their principle.	**L3**
CO2	Familiar with Design considerations of fiber optic systems.	**L3**
CO3	To perform characteristics of optical fiber, sources and detectors, design as well as conduct experiments in software and hardware, analyze the results to provide valid conclusions.	**L3**
CO4	Apply the principles of atomic physics to materials used in optics and photonics;	**L3**
CO5	Calculate properties of and design modern optical fibres and photonic crystals;	**L5**
CO6	Use the tools, methodologies, language and conventions of physics to test and communicate ideas and explanations;	**L5**
CO7	Integrate several components of the course in the context of a new situation (unique to postgraduate coursework).	**L4**

***Note**: L1- Remember, L2 – Understand, L3 – Apply, L4 – Analyze, L5 – Evaluate, L6 – Create*

COURSE CONTENTS

UNIT-I: Laser systems

General description, Laser structure, Single mode laser theory, Excitation mechanism and working of: CO2, Nitrogen, Argonion, Excimer, X-ray, Free-electron, Dye, Nd: YAG, Alexanderite and Ti: sapphire lasers, Diode pumped solid state laser, Optical parametricoscillator (OPO) lasers. Optical amplifiers- Semiconductor optical amplifiers, Erbium doped wave guide optical amplifiers, Raman amplifiers, Fiber Lasers. Laser Applications-Lasers in Isotope separation, Laser inter ferometry and speck lemetrology, Velocity measurements.

UNIT-II: Properties of Laser Radiation

Introduction, Laser line width, Laser frequency stabilization, Beam divergence, Beam coherence, Brightness, Focusing properties of laser radiation, Q-switching, Methods of Q-switching : Rotating-mirror method, Electro-optic Q-switching, Acoustic-optic Q-switching and Passive Q-switching, Mode locking, Methods of mode locking: Active and passive mode locking techniques, Frequency doubling and Phase conjugation

UNIT-III: Opto-electronic Devices -I

Introduction, P-N junction diode, Carrier recombination and diffusion in P-N junction, Injection efficiency, Internal quantum efficiency, Hetero-junction, Doublehetero-junction, Quantum well, Quantumdot and Super lattices; LED materials, Device configuration and efficiency.

UNIT-IV: Opto-electronic Devices-II

Light extraction from LEDs, LED structures-single hetero structures, double hetero structures, Device performances and applications, Quantum welllasers; Photo diode and Avalanche photodiodes(APDs), Laser Diodes-Amplification, Feedback and oscillation, Power and efficiency, Spectral and spatial characteristics.

UNIT–V: Modulation of Light

Introduction, Birefringence, Electro-optic effect, Pockels and Kerr effects, Electro-optic Phase modulation, Electro-optic amplitude modulation, Electro-optic modulators: scanning and switching, Acousto-optic effect, Acousto-optic modulation, Raman-Nath and Bragg modulators: deflectors and spectrum analyzer, Magneto-optic effect, Faraday rotatoras an optical isolator. Advantages of optical modulation.

Text books:

1. Lasers: Principles and applications by J. Wilson And J.F.B. Hawkes, Prentice, Hall of India, New Delhi, 1996.
2. Laser fundamentals, W.T. Silfvast, Foundation books, New Delhi, 1999.
3. Semi conductor opto electronics devices, P. Bhattacharya, Prentice –Hall of India, New Delhi, 1995.17

Reference Books:

1. Optical fiber communications, John M. Senior, Prentice-Hall of India, New Delhi, 2001
2. Optoelectronics: An Introduction, J. Wilson and J.F.B. Hawkes, Prentice-Hall of India, New Delhi, 1996.
3. Electro-Optical devices, M.A. Karim, Boston, Pws-Kent Publishers, 1990

RESEARCH METHODOLOGY and IPR (23MTVLT03)

Course Category		Credits	**2**
Course Type	**Theory**	L-T-P	**2-0-2**
Year	**I**	CIE Marks	**25**
Sem.	**I**	SEE Marks	**75**
		Total Marks	**100**

Course Outcomes:

At the end of course, the student will be able to

Number	COURSE OUTCOMES (COs)	Blooms Taxonomy
CO1	Understand research problem formulation.	**L2**
CO2	Analyze research related information	**L2**
CO3	Follow research ethics	**L2**
CO4	Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.	**L2**
CO5	Understanding that when IPR would take such important place in growth of individuals &nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.	**L2**
CO6	Understand that IPR protection provides an incentive to in ventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.	**L2**

***Note**: L1- Remember, L2 – Understand, L3 – Apply, L4 – Analyze, L5 – Evaluate, L6 – Create*

COURSE CONTENTS

UNIT-1:

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT-2:

Effective literature studies approaches, analysis Plagiarism, Research ethics. Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by are view committee

UNIT-3:

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT4:

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and data bases. Geographical Indications.

UNIT5:

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

Text Books:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students‘"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
3. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
4. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd, 2007.

Reference Books:

1. Mayall, "Industrial Design", McGrawHill,1992.
2. Niebel, "Product Design", McGraw Hill, 1974.
3. Asimov, "Introduction to Design", Prentice Hall, 1962
4. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in Ne
5. Technological Age", 2016.
6. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

CMOS ANALOG IC DESIGN LAB (23MTVLL01)

Course Category	**LAB-1**	Credits	**2**
Course Type	**Theory**	L-T-P	**0-0-4**
Year	**I**	CIE Marks	**25**
Sem.	**I**	SEE Marks	**75**
		Total Marks	**100**

Course Objectives:

- The students are required to design and implement any TEN Experiments using CMOS130nm Technology with Mentor Graphics Tool/Cadence/Synopsys/ Industry Equivalent Standard Software.
- The students are required to implement LAYOUTS of any SIX Experiments using CMOS130nm Technology with Mentor Graphics Tool/Cadence/Synopsys/ Industry Equivalent Standard Software. And Compare the results with Pre-Layout Simulation.

Course Outcomes:

At the end of course, the student will be able to

Number	COURSE OUTCOMES (COs)	Blooms Taxonomy
CO1	Have the ability to explain the VLSI Design Methodologies using Mentor Graphics Tools	**L3**
CO2	Grasp the significance of various cmos analog circuits in full-custom IC Design flow	**L4**
CO3	Have the ability to explain the Physical Verification in Layout Design	**L4**
CO4	Fully Appreciate the design and analyze of analog and mixed signal simulation	**L4**
CO5	GrasptheSignificanceofPre-LayoutSimulationandPost-LayoutSimulation	**L4**

***Note**: L1- Remember, L2 – Understand, L3 – Apply, L4 – Analyze, L5 – Evaluate, L6 – Create*

List of Experiments:

1. MOS Device Characterization and parametric analysis
2. Common Source Amplifier
3. Common Source Amplifier with sourced generation
4. Cas code amplifier
5. Simple current mirror
6. Cas code current mirror.
7. Wilson current mirror.
8. Differential Amplifier
9. Operational Amplifier
10. Sample and Hold Circuit
11. Direct-conversion ADC
12. R-2R Ladder Type DAC

Lab Requirements:

Software:

Mentor Graphics – Pyxis Schematic, IC Station, Calibre, ELDO Simulator

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

CMOS DIGITAL IC DESIGN LAB (23MTVLL02)

Course Category	**LAB-2**	Credits	**2**
Course Type	**Theory**	L-T-P	**0-0-4**
Year	**I**	CIE Marks	**25**
Sem.	**I**	SEE Marks	**75**
		Total Marks	**100**

Course Objectives:

- The student sare required to design and implement the Circuit and Layout of any TEN Experiments using CMOS130nm Technology with Mentor Graphics Tool/Cadence/Synopsys/Industry Equivalent Standard Software.

Course Outcomes:

At the end of course, the student will be able to

Number	COURSE OUTCOMES (COs)	Blooms Taxonomy
CO1	Have the ability to explain the VLSI Design Methodologies using Mentor Graphics Tools	**L3**
CO2	Grasp the significance of various design logic Circuits in full – custom IC Design.	**L4**
CO3	Have the ability to explain the Physical Verification in Layout Extraction	**L4**
CO4	Fully Appreciate the design and analyze of CMOS Digital Circuit	**L4**
CO5	Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation	**L4**

***Note**: L1- Remember, L2 – Understand, L3 – Apply, L4 – Analyze, L5 – Evaluate, L6 – Create*

List of Experiments:

1. Inverter Characteristics.
2. NAND and NOR Gate
3. XOR and XNOR Gate
4. 2:1Multiplexer
5. Full Adder
6. RS-Latch
7. Clock Divider
8. JK- FlipFlop
9. Synchronous Counter
10. Asynchronous Counter
11. Static RAM Cell
12. Dynamic Logic Circuits
13. Linear Feedback Shift Register

Lab Requirements:

Software:

Mentor Graphics Tool / Cadence / Synopsys / Industry Equivalent Standard Software

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

MIXED SIGNAL & RF IC DESIGN (23MTVLT04)

Course Category	**PC**	Credits	**3**
Course Type	**Theory**	L-T-P	**3-0-0**
Year	**I**	CIE Marks	**25**
Sem.	**II**	SEE Marks	**75**
		Total Marks	**100**

Course Objectives:

- To understand the design of basic cells like Op-Amp, against process and temperature variations meeting the mixed signal specifications.
- To be able to design comparators that can meet the high speed requirements of digital circuitry.
- To be able to design a complete mixed signal system that includes efficient data conversion and RF circuits with minimizing switching.
- To understand the design bottlenecks specific to RF IC design, linearity related issues, and ISI.
- To have a comprehensive idea about different multiple access techniques, wireless standards and various transceiver architectures

Course Outcomes:

At the end of course, the student will be able to

Number	**COURSE OUTCOMES (COs)**	**Blooms Taxonomy**
CO1	Design basic cells like Op-Amp, against process and temperature variations meeting the mixed signal specifications	**L3**
CO2	Design comparators that can meet the high speed requirements of digital circuitry.	**L4**
CO3	Design a complete mixed signal system that includes efficient data conversion and RF circuits with minimizing switching.	**L3**
CO4	Understand the design bottlenecks specific to RF IC design, linearity related issues and ISI	**L2**
CO5	Comprehend different multiple access techniques, wireless standards and various transceiver architectures	**L4**

Note: *L1- Remember, L2 – Understand, L3– Apply, L4 – Analyze, L5 – Evaluate, L6 – Create*

COURSE CONTENTS

UNIT - I

Basic Building Blocks, Op-Amp, Capacitors, Switches, Non-overlapping Clocks, Basic Operation and Analysis, Resistor Equivalence of a Switched Capacitor, Parasitic-Sensitive Integrator, Parasitic-Insensitive Integrators, Signal-Flow-Graph Analysis, Noise in Switched-Capacitor Circuit

UNIT - II:

Ideal D/A Converter, Ideal A/D Converter, Quantization Noise, Deterministic Approach, Stochastic Approach, Signed Codes, Performance Limitations, Resolution, Offset and Gain Error, Accuracy and Linearity Integrating Converters, Successive-Approximation Converters, DAC-Based Successive Approximation, Charge-Redistribution A/D, Resistor-Capacitor Hybrid, Speed Estimate for Charge-Redistribution Converters, Error Correction in Successive-Approximation Converters

UNIT - III:

Basic Phase-Locked Loop Architecture, Voltage Controlled Oscillator, Divider Phase Detector, Loop Filer, The PLL in Lock, Linearized Small-Signal Analysis, Second-Order PLL Model, Limitations of the Second-Order Small-Signal Model, PLL Design Example, Jitter and Phase Noise, Period Jitter, P-Cycle Jitter, Adjacent Period Jitter, other Spectral Representations of Jitter, Probability Density Function of Jitter, Ring Oscillators , LC Oscillators , phase Noise of Oscillators, jitter and Phase Noise in PLLS

UNIT - IV:

INTRODUCTION TO RF AND WIRELESS TECHNOLOGY: Complexity comparison, Design bottle necks, Applications, Analog and digital systems, Choice of Technology. BASICCONCEPTS IN RF DESIGN: Nonlinearity and time variance, ISI, Random process and noise, sensitivity and dynamic range, passive impedance transformation.

UNIT - V:

Multiple Access: Techniques and wireless standards, mobile RF communication, FDMA, TDMA, CDMA, Wireless standards.

Transceiver Architectures: General considerations, receiver architecture, Transmitter Architecture, transceiver performance tests, case studies.

Amplifiers, Mixers And Oscillators: LNAs, down conversion mixers, Cascaded Stages, oscillators, Frequency synthesizers.

Text Books:

1. David A Johns, Ken Martin: Analog IC design, Wiley 2008.
2. R Gregorian and G C Temes: Analog MOS integrated circuits for signal processing, Wiley 1986

Reference Books:

1. Roubik Gregorian: Introduction to CMOS Op-amps and comparators, Wiley, 2008.
2. Behzad Razavi, RF Microelectronics Prentice Hall of India, 2001
3. Thomas H. Lee, The Design of CMOS Radio Integrated Circuits, Cambridge University Press.

PHYSICAL DESIGN AUTOMATION (23MTVLT05)

Course Category	**PC**	Credits	**3**
Course Type	**Theory**	L-T-P	**3-0-0**
Year	**I**	CIE Marks	**25**
Sem.	**II**	SEE Marks	**75**
		Total Marks	**100**

Course Objectives:

- To understand the relationship between design automation algorithms and various constraints posed by VLSI fabrication and design technology.
- To learn the design algorithms to meet the critical design parameters.
- To know the layout optimization techniques and map them to the algorithms
- To understand proto-type EDA tools and know how to test its efficacy

Course Outcomes

At the end of course, the student will be able to

Number	**COURSE OUTCOMES (COs)**	**Blooms Taxonomy**
CO1	Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS, Alternative CMOS Logics, Estimation of Delay and Power, Adders Design.	**L3**
CO2	Classify different semiconductor memories.	**L3**
CO3	Analyze, design and implement combinational and sequential MOS logic circuits.	**L4**
CO4	Analyze complex engineering problems critically in the domain of digital IC design for conducting research.	**L4**
CO5	Solve engineering problems for feasible and optimal solutions in the core area of digital ICs.	**L5**

Note: *L1- Remember, L2 – Understand, L3– Apply, L4 – Analyze, L5 – Evaluate, L6 – Create*

COURSE CONTENTS

UNIT -I

VLSI design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication, Design styles: full custom, standard cell, gate arrays, field programmable gate arrays, sea of gates and comparison, system packaging styles, multi-chip modules. Design rules, layout of basic devices, fabrication process and its impact on physical design, interconnect delay, noise and cross talk, yield and fabrication cost.

UNIT -II:

Factors, Complexity Issues and NP-hard Problems, Basic Algorithms (Graph and Computational Geometry): graph search algorithms, spanning tree algorithms, shortest path algorithms, matching algorithms, min-cut and max-cut algorithms, Steiner tree algorithms

UNIT -III:

Basic Data Structures, atomic operations for layout editors, linked list of blocks, bin based methods, neighbour pointers, corner stitching, multi-layer operations.

UNIT -IV:

Graph algorithms for physical design: classes of graphs, graphs related to a set of lines, graphs related to set of rectangles, graph problems in physical design, maximum clique and minimum coloring, maximum k-independent set algorithm, algorithms for circle graphs.

UNIT -V:

Partitioning algorithms: design style specific partitioning problems, group migrated algorithms, simulated annealing and evolution, and Floor planning and pin assignment, Routing and placement algorithms

Text Books:

1. Naveed Shervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic, 1999.
2. Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2008

DESIGN FOR TESTABILITY (23MTVLE07)

Course Category	**PE/ELECTIVE-III**	Credits	**3**
Course Type	**Theory**	L-T-P	**3-0-0**
Year	**I**	CIE Marks	**25**
Sem.	**II**	SEE Marks	**75**
		Total Marks	**100**

Course Outcomes:

At the end of course, the student will be able to

Number	COURSE OUTCOMES (COs)	Blooms Taxonomy
CO1	Demonstrate advanced knowledge in The basic faults that occur in digital systems, Testing of stuck at faults for digital circuits, Design for testability.	**L2**
CO2	Analyze testing issues in the field of digital system design critically for conducting research.	**L3**
CO3	Solve engineering problems by modeling different faults for fault free simulation in digital circuits.	**L3**
CO4	Apply appropriate research methodologies and techniques to develop new testing strategies for digital and mixed signal circuits and systems.	**L4**

Note: *L1- Remember, L2 – Understand, L3– Apply, L4 – Analyze, L5 – Evaluate, L6 – Create*

COURSE CONTENTS

UNIT -I

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT -II:

Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation.

UNIT -III:

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT -IV:

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per Scan BIST Systems, Circular Self-Test Path System, Memory BIST, Delay Fault BIST.

UNIT -V:

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

Text Books:

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits -M.L. Bushnell, V. D. Agrawal, Kluwer Academic Publishers.

Reference Books:

1. Digital Systems and Testable Design - M. Abramovici, M.A. Breuer and A.D Friedman, Jaico Publishing House.
2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

IOT AND ITS APPLICATIONS (23MTVLE08)

Course Category	PE/ELECTIVE-III	Credits	**3**
Course Type	Theory	L-T-P	**3-0-0**
Year	I	CIE Marks	**25**
Sem	II	SEE Marks	**75**
		TOTAL MARKS	**100**

COURSE OUTCOMES

At the end of course, the student will be able to

Number	COURSE OUTCOMES (COs)	Blooms Taxonomy
CO1	Apply the Knowledge in IOT Technologies and Data management	**L2**
CO2	Determine the values chains Perspective of M2M to IOT.	**L2**
CO3	Implement the state of the Architecture of an IOT.	**L3**
CO4	Compare IOT Applications in Industrial & real world..	**L4**
CO5	Demonstrate knowledge and understanding the security and ethical issues of an IOT.	**L4**

Note: *L1- Remember, L2 – Understand, L3– Apply, L4 – Analyze, L5 – Evaluate, L6 – Create*

COURSE CONTENTS

UNIT I:

Fundamentals of IoT- Evolution of Internet of Things, Enabling Technologies, IoT Architectures,oneM2M, IoT World Forum (IoTWF) and Alternative IoT models, Simplified IoT Architecture and Core IoT Functional Stack, Fog, Edge and Cloud in IoT, Functional blocks of an IoT ecosystem, Sensors, Actuators, Smart Objects and Connecting Smart Objects.

IoT Platform overview: Overview of IoT supported Hardware platforms such as: Raspberry pi, ARM Cortex Processors, Arduino and Intel Galileo boards.

UNIT II:

IoT Protocols- IT Access Technologies: Physical and MAC layers, topology and Security of IEEE 802.15.4, 802.15.4g, 802.15.4e, 1901.2a, 802.11ah and Lora WAN, Network Layer: IP versions, Constrained Nodes and Constrained Networks, Optimizing IP for IoT: From 6LoWPAN to 6Lo, Routing over Low Power and Lossy Networks, Application Transport Methods: Supervisory Control and Data Acquisition, Application Layer Protocols: CoAP and MQTT.

UNIT III:

Design And Development- Design Methodology, Embedded computing logic, Microcontroller, System on Chips, IoT system building blocks, Arduino, Board details, IDE programming, Raspberry Pi, Interfaces and Raspberry Pi with Python Programming.

UNIT IV:

Data Analytics And Supporting Services- Structured Vs Unstructured Data and Data in Motion Vs Data in Rest, Role of Machine Learning – No SQL Databases, Hadoop Ecosystem, Apache Kafka, Apache Spark, Edge Streaming Analytics and Network Analytics, Xively Cloud for IoT, Python Web Application Framework, Django, AWS for IoT, System Management with NETCONF-YANG

UNIT V:

Case Studies/Industrial Applications: IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipments. Use of Big Data and Visualization in IoT, Industry 4.0 concepts.

Sensors and sensor Node and interfacing using any Embedded target boards (Raspberry Pi / Intel Galileo/ARM Cortex/ Arduino)

Text Books:

1. IoT Fundamentals: Networking Technologies, Protocols and Use Cases for Internet of Things, David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Rob Barton and Jerome Henry, Cisco Press, 2017

Reference Books:

1. Internet of Things – A hands-on approach, ArshdeepBahga, Vijay Madisetti, Universities Press, 2015
2. The Internet of Things – Key applications and Protocols, Olivier Hersent, David Boswarthick, Omar Elloumi and Wiley, 2012 (for Unit 2).
3. "From Machine-to-Machine to the Internet of Things – Introduction to a New Age of Intelligence", Jan Ho¨ ller, Vlasios Tsiatsis, Catherine Mulligan, Stamatis, Karnouskos, Stefan Avesand. David Boyle and Elsevier, 2014.
4. Architecting the Internet of Things, Dieter Uckelmann, Mark Harrison, Michahelles and Florian (Eds), Springer, 2011.
5. Recipes to Begin, Expand, and Enhance Your Projects, 2nd Edition,Michael Margolis, Arduino Cookbook and O"Reilly Media, 2011.

VLSI SIGNAL PROCESSING (23MTVLE09)

Course Category	**PE/ELECTIVE-III**	Credits	**3**
Course Type	**Theory**	L-T-P	**3-0-0**
Year	**I**	CIE Marks	**25**
Sem.	**II**	SEE Marks	**75**
		Total Marks	**100**

Course Outcomes:

At the end of course, the student will be able to

Number	**COURSE OUTCOMES (COs)**	**Blooms Taxonomy**
CO1	Ability to modify the existing or new DSP architectures suitable for VLSI.	**L2**
CO2	Understand the concepts of folding and unfolding algorithms and applications.	**L2**
CO3	Ability to implement fast convolution algorithms.	**L2**
CO4	Low power design aspects of processors for signal processingand wireless applications.	**L4**

Note: *L1- Remember, L2 – Understand, L3– Apply, L4 – Analyze, L5 – Evaluate, L6 – Create*

COURSE CONTENTS

UNIT - I

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processingfor Low Power Retiming Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques

UNIT – II

Folding and Unfolding: Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multirate systems Unfolding- Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding

UNIT - III

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT - IV

Fast Convolution: Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT - V:

Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic. Numerical strength reduction, synchronous, wave and asynchronous pipe lines, low power design. Low Power Design: Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches

Text Books:

1. Keshab K. Parthi [A1] , VLSI Digital signal processing systems, design and implementation[A2] , Wiley, Inter Science, 1999.
2. Mohammad Isamail and Terri Fiez, Analog VLSI signal and information processing, McGraw Hill, 1994
3. S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, Prentice Hall, 1985.

NETWORK SECURITY AND CRYPTOGRAPHY (23MTVLE10)

Course Category	**PE/ELECTIVE-IV**	Credits	**3**
Course Type	**Theory**	L-T-P	**3-0-0**
Year	**I**	CIE Marks	**25**
Sem.	**II**	SEE Marks	**75**
		Total Marks	**100**

Course Outcomes:

At the end of course, the student will be able to

Number	COURSE OUTCOMES (COs)	Blooms Taxonomy
CO1	Identify and utilize different forms of cryptography techniques.	**L2**
CO2	Incorporate authentication and security in the network applications.	**L2**
CO3	Distinguish among different types of threats to the system and handle the same.	**L4**

Note: *L1- Remember, L2 – Understand, L3 – Apply, L4 – Analyze, L5 – Evaluate, L6 – Create*

COURSE CONTENTS

UNIT 1: Security

Need, security services, Attacks, OSI Security Architecture, one time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transpositionciphers, Cryptanalysis of Classical Encryption Techniques.

Number Theory

Introduction, Fermat‟s and Euler‟s Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

UNIT 2: Private-Key (Symmetric) Cryptography

Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and

Differential Cryptanalysis.

UNIT 3: Public-Key (Asymmetric) Cryptography

RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

UNIT 4: Authentication

IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer and Transport Layer Security, Secure Electronic Transaction.

UNIT 5: System Security

Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Counter measures, Firewalls, Firewall Design Principles, Trusted Systems.

Text Books:

1. William Stallings, "Cryptography and Network Security, Principles and Practices", Pearson Education, 3rd Edition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private
3. Communication in a Public World", Prentice Hall, 2nd Edition

Reference Books:

1. Christopher M. King, Ertem Osmanoglu, Curtis Dalton, "Security Architecture, Design Deployment and Operations", RSA Pres,
2. Stephen Northcutt, Leny Zeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey,
3. "Inside Network Perimeter Security", Pearson Education, 2nd Edition
4. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident

MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS (23MTVLE11)

Course Category	**PE/ELECTIVE-IV**	Credits	**3**
Course Type	**Theory**	L-T-P	**3-0-0**
Year	**I**	CIE Marks	**25**
Sem.	**II**	SEE Marks	**75**
		Total Marks	**100**

Course Outcomes:

At the end of course, the student will be able to

Number	COURSE OUTCOMES (COs)	Blooms Taxonomy
CO1	Compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.	**L2**
CO2	Identify and characterize architecture of Programmable DSP Processors	**L4**
CO3	Develop small applications by utilizing the ARM processor core and DSP processor based platform.	**L3**

Note: *L1- Remember, L2 – Understand, L3 – Apply, L4 – Analyze, L5 – Evaluate, L6 – Create*

COURSE CONTENTS

UNIT 1:

ARM Cortex-M3 processor: Applications, Programming model – Registers,

Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces

UNIT 2:

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.

UNIT 3:

LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other Serial interfaces, PWM, RTC, WDT

UNIT 4:

Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family

UNIT 5:

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations Code Composer Studio for application development for digital signal processing, On chip peripherals, Processor benchmarking

Text Books:

1. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition
2. Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture, Programming and Applications", TMH, 2nd Edition
3. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publication

Reference Books:

1. Steve furber, "ARM System-on-Chip Architecture", Pearson Education
2. Frank Vahid and Tony Givargis, "Embedded System Design", Wiley
3. Technical references and user manuals on www.arm.com, NXP Semi conductor www.nxp.com and Texas Instruments www.ti.com

LOW POWER VLSI DESIGN (23MTVLE12)

Course Category	**PE/ELECTIVE-IV**	Credits	**3**
Course Type	**Theory**	L-T-P	**3-0-0**
Year	**I**	CIE Marks	**25**
Sem.	**II**	SEE Marks	**75**
		Total Marks	**100**

Course Outcomes:

At the end of course, the student will be able to

Number	**COURSE OUTCOMES (COs)**	**Blooms Taxonomy**
CO1	Identify the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability.	**L3**
CO2	Characterize and model power consumption & understand the basic analysis methods.	**L3**
CO3	Understand leakage sources and reduction techniques.	**L3**

Note: *L1- Remember, L2 – Understand, L3– Apply, L4 – Analyze, L5 – Evaluate, L6 – Create*

COURSE CONTENTS

UNIT-I: Sources of Power Dissipation

Introduction, Short-Circuit Power Dissipation, Switching Power Dissipation, Dynamic Power for a Complex Gate, Reduced Voltage Swing, Switching Activity, Leakage Power Dissipation, p–n Junction Reverse-Biased Current, Band-to-Band Tunneling Current, Sub threshold Leakage Current, Short-Channel Effects

UNIT 2: Supply Voltage Scaling for Low Power

Device Feature Size Scaling, Constant-Field Scaling, Constant-Voltage Scaling, Architectural-Level Approaches: Parallelism for Low Power, Pipelining for Low Power, Combining Parallelism with Pipelining, Voltage Scaling Using High-Level Transformations: Multilevel Voltage Scaling Challenges in MVS Voltage Scaling Interfaces, Static Timing Analysis Dynamic Voltage and Frequency Scaling

UNIT-3: Switched Capacitance Minimization

Probabilistic Power Analysis: Random logic signals, probability and frequency, probabilistic power analysis techniques, signal entropy, Bus Encoding: Gray Coding, One-Hot Coding, Bus-Inversion, T0 Coding, Clock Gating, Gated-Clock FSMs FSM State Encoding, FSM Partitioning, Pre computation, Glitching Power Minimization

UNIT 4: Leakage Power Minimization

Fabrication of Multiple Threshold Voltages, Multiple Channel Doping, Multiple Oxide CMOS, Multiple Channel Length, Multiple Body Bias, VTCMOS Approach, MTCMOS Approach, Power Gating, Clock Gating Versus Power Gating, Power-Gating Issues, Isolation Strategy, State Retention Strategy, Power-Gating Controller, Power Management, Combining DVFS and Power Management

UNIT 5: Low power clock distribution & Simulation Power Analysis

Low power clock distribution: Power dissipation in clock distribution, single driver versus distributed buffers, Zero skew versus tolerable skew, chip and package co design for clock network.

Simulation Power Analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, architecture level analysis, data correlation analysis of DSP systems, Monte Carlo Simulation

Text Books:

1. Low-Power VLSI Circuits and Systems, Ajit Pal, SPRINGER PUBLISHERS
2. Practical Low Power Digital VlsiDesign, Gary Yeap Motorola, Springer Science Business Media, LLC.

Reference Books:

1. Low Power CMOS Design – Anantha Chandrakasan, IEEE Press/Wiley International, 1998.
2. Massoud Pedram, Jan M. Rabaey, "Low power design methodologies", Kluwer Academic Publishers.
3. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.

MIXED SIGNAL IC DESIGN LAB (23MTVLL04)

Course Category	**LAB-3**	Credits	**2**
Course Type	**Theory**	L-T-P	**0-0-4**
Year	**I**	CIE Marks	**25**
Sem.	**II**	SEE Marks	**75**
		Total Marks	**100**

Detailed Syllabus:

Cycle 1:

1) Fully compensated op-amp with resistor and miller compensation
2) High speed comparator design
   i. Two stage cross coupled clamped comparator
   ii. Strobed Flip-flop
3) Data converter

Cycle 2:

1) Switched capacitor circuits
   i. Parasitic sensitive integrator
   ii. Parasitic insensitive integrator
2) Design of PLL
3) Design of VCO
4) Bandgap reference circuit
5) Layouts of All the circuits Designed and Simulated

Software:

Mentor Graphics/ Cadence/ Tanner/Industry Equivalent Standard Software Tools

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

Reading:

1) David A johns, Ken Martin, Analog Integrated Circuit Design, Wiley, 2008.
2) R. Gregorian and G.C Ternes, Analog MOS Integrated Circuits for Signal Processing, Wiley, 1986.
3) Roubik Gregorian, Introduction to CMOS OpAmp and Comparators, Wiley, 1999.
4) Alan Hastlings, The art of Analog Layout, Wiley, 2005.

PHYSICAL DESIGN AUTOMATION LAB (23MTVLL05)

Course Category	**LAB-4**	Credits	**2**
Course Type	**Theory**	L-T-P	**0-0-4**
Year	**I**	CIE Marks	**25**
Sem.	**II**	SEE Marks	**75**
		Total Marks	**100**

Detailed Syllabus:

Cycle 1:

1) Graph algorithms

a) Graph search algorithms

i. Depth first search

ii. Breadth first search

b) Spanning tree algorithm

i. Kruskal"s algorithm

c) Shortest path algorithm

i. Dijkstra algorithm

ii. Floyd- Warshall algorithm

d) Steiner tree algorithm

2) Computational geometry algorithm

a) Line sweep method

b) Extended line sweep method

Cycle 2:

3) Partitioning algorithms

I) Group migration algorithms

a) Kernighan –Lin algorithm

b) Extensions of Kernighan-Lin algorithm

i) Fiduccias –Mattheyses algorithm

ii) Goldberg and Burstein algorithm

II) Simulated annealing and evolution algorithms

a) Simulated annealing algorithm

b) Simulated evolution algorithm

III) Metric allocation method

4) Floor planning algorithms

i) Constraint based methods

ii) Integer programming based methods

iii) Rectangular dualization based methods

iv) Hierarchical tree based methods

v) Simulated evolution algorithms

vi) Time driven Floorplanning algorithms

5) Routing algorithms

I) Two terminal algorithms

a) Maze routing algorithms

i) Lee‟s algorithm

ii) Soukup‟s algorithm

iii) Hadlock algorithm

b) Line-Probe algorithm

c) Shortest path based algorithm

II) Multi terminal algorithm

a) Stenier tree based algorithm

i) SMST algorithm

ii) Z-RST algorithm

Software required: C/C++ Programming Language /Relevant software

Reading:

1) Naveed Shervani, Algorithms for Physical Design Automation, 3rd Edition, Kluwer Academic, 1998.
2) Charles J Alpert, Dinesh P Mehta, Sachin S. Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2008.

MINI PROJECT (23MTVLP01)

Course Category	**LAB-4**	Credits	**2**
Course Type	**Theory**	L-T-P	**0-0-4**
Year	**I**	CIE Marks	**25**
Sem.	**II**	SEE Marks	**75**
		Total Marks	**100**

Syllabus Contents:

- The students are required to search / gather the material / information on a specific a topic comprehend it and present / discuss in the class.

Course Outcomes:

At the end of this course, students will be able to

Number	COURSE OUTCOMES (COs)	Blooms Taxonomy
CO1	Understand of contemporary / emerging technology for various processes and systems.	**L2**
CO2	Share knowledge effectively in oral and written form and formulate documents	**L3**

Note: *L1- Remember, L2 – Understand, L3– Apply, L4 – Analyze, L5 – Evaluate, L6 – Create*

SEMESTER-WISE COURSE STRUCTURE

Semester-III **M.Tech. (VLSI)**

S.No	Course Code	Course Name	L	T	P	Credits
1	23MTVLE13 23MTVLE14 23MTVLE15	**Professional Elective 5:** 1.Scripting Languages for VLSI 2. Digital System Design & Verification 3. Hardware Software co-design	3	0	0	3
2	23MTVLOE1 23MTVLOE2 23MTVLOE3 23MTVLOE4 23MTVLOE5 23MTVLOE6	**Open Elective:** 1. Business Analytics 2. Industrial Safety 3. Operations Research 4. Cost Management of Engineering Projects 5. Composite Materials 6. Waste to Energy	3	0	0	3
3	23MTVLP02	Dissertation Phase -I /Industrial Project **(to be continued and evaluated next semester)**	0	0	20	10#
			Total			**16**

Category		Credits
PE	Professional Elective	3
OE	Open Elective	3
	Dissertation	10
Total Credits		**16**

#Evaluated and Displayed in IV Semester Marks list.

*Students going for Industrial Project/Thesis will complete these courses through MOOCs

Semester-IV **M.Tech. (VLSI)**

S.No	Course Code	Course Name	L	T	P	Credits
1	23MTVLP03	Project/ Dissertation Phase-II **(continued from III semester)**	0	0	32	16
			Total			**16**

Audit Course 1& 2

1. English for Research Paper Writing
2. Disaster Management
3. Sanskrit for Technical Knowledge
4. Value Education
5. Constitution of India
6. Pedagogy Studies
7. Stress Management by Yoga
8. Personality Development through Life Enlightenment Skills

SCRIPTING LANGUAGES FOR VLSI (23MTVLE13)

(Elective V)

Course Category	**PE/ELECTIVE-V**	Credits	**3**
Course Type	**Theory**	L-T-P	**3-0-0**
Year	**II**	CIE Marks	**25**
Sem.	**I**	SEE Marks	**75**
		TOTAL MARKS	**100**

Course Outcomes

At the end of course, the student will be able to

Number	COURSEOUT COMES (COs)	Blooms Taxonomy
CO1	Gaiznfluency in programming with scripting languages	**L3**
CO2	Create and run scripts using PERL/TCL/PYTHON in CAD Tools	**L5**
CO3	Demonstrate the use of PERL/PYTHON/TCL in developing system and web applications	**L3**

Note: *L1-Remember, L2–Understand, L3–Apply, L4–Analyze, L5 –Evaluate, L6 –Create*

COURSE CONTENTS

UNIT-I:

Introduction to Scripts and Scripting: Basics of Linux, Origin of Scripting languages, scriptingtoday, Characteristics and uses of scripting languages.

ERL: Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT-II:

Advanced PERL: Finer points of Looping, Subroutines, Using Pack and Unpack, working with files, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, tied variables, interfacing to the operating systems, Security issues.

UNIT-III:

TCL: The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT-IV:

Advanced TCL: The eval, source, exec and up-level commands, Libraries and packages, Namespaces, trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, TCL and TK integration.

UNIT-V:

PYTHON: Introduction to PYTHON language, PYTHON-syntax, statements, functions, Built-in functions and Methods, Modules in PYTHON, Exception Handling.

Text Books:

1. The World of Scripting Languages- David Barron, Wiley Student Edition, 2010.
2. PYTHON Web Programming, Steve Holden and David Beazley, New Riders Publications

References:

1. TCL/TK: A Developer's Guide-ClifFlynt,2003, Morgan Kaufmann Series.
2. Core PYTHON Programming, Chun, Pears on Education, 2006.
3. Learning Perl, Randal L. Schwartz, O "Reilly publications 6th edition 2011.
4. Linux: The Complete Reference", Richard Peterson McGraw Hill Publications, 6th Edition, 2008.

DIGITAL SYSTEM DESIGN & VERIFICATION (23MTVLE14)
(Elective V)

Course Category	**PE/ELECTIVE-V**	Credits	**3**
Course Type	**Theory**	L-T-P	**3-0-0**
Year	**II**	CIE Marks	**25**
Sem.	**I**	SEE Marks	**75**
		TOTAL MARKS	**100**

Course Outcomes

At the end of course, the student will be able to

Number	COURSEOUTCOMES(COs)	Blooms Taxonomy
CO1	Familiarity of Frontend design and verification techniques and create reusable test environments.	**L5**
CO2	Verify increasingly complex designs more efficiently and effectively	**L5**
CO3	Use EDA tools like Cadence, Mentor Graphics.	**L6**

Note: *L1-Remember, L2–Understand, L3–Apply, L4–Analyze, L5 –Evaluate, L6 –Create*

COURSE CONTENTS

UNIT 1

Revision of basic Digital systems: Combinational Circuits, Sequential Circuits, Logic families. Synchronous FSM and asynchronous design, Meta-stability, Clock distribution and issues, basic building blocks like PWM module, pre-fetch unit, programmable counter, FIFO, Booth's multiplier, ALU, Barrel shifter etc.

UNIT 2

Verilog/VHDL Comparisons and Guidelines, Verilog: HDL fundamentals, simulation, and test bench design, Examples of Verilog codes for combinational and sequential logic, Verilog AMS. IP and Prototyping: IP in various forms: RTL Source code, Encrypted Source code, Soft IP, Netlist, Physical IP, and Use of external hard IP during prototyping, Case studies, and Speed issues.

UNIT 3

System Verilog and Verification: Verification guidelines, Datatypes, procedural statements and routines, connecting the test bench and design, Assertions, Basic OOP concepts, Randomization. Testing of logic circuits: Fault models, BIST, JTAG interface Introduction to basic scripting language: Perl, Tcl/Tk

UNIT 4

Current challenges in physical design: Roots of challenges, Delays: Wire load models Generic PDflow, Challenges in PD flow at different steps, SI Challenge - Noise & Crosstalk, IR Drop, Process effects: Process Antenna Effect &Electro migration

UNIT 5

Programmable Logic Devices: Introduction, Evolution: PROM, PLA, PAL, Architecture of PAL's, Applications, Programming PLD's, FPGA with technology: Anti-fuse, SRAM, EPROM, MUX, FPGA structures, and ASIC Design Flows, Programmable Interconnections, Coarse grained reconfigurable devices

Text Books:

1. Douglas Smith, “HDL Chip Design: A Practical Guide for Designing, Synthesizing &
2. Simulating ASICs & FPGAs Using VHDLor Verilog”, Doone publications, 1998.
3. Samir Palnitkar, “Verilog HDL: A guide to Digital Design and Synthesis”, Prentice Hall, 2nd Edition, 2003.

Reference Books:

1. Doug Amos, Austin Lesea, Rene Richter, “FPGA based Prototyping Methodology Manual”, Synopsys Press, 2011.
2. Christophe Bobda, “Introduction to Reconfigurable Computing, Architectures, Algorithms and Applications”, Springer, 2007.
3. Janick Bergeron, “Writing Test benches: Functional Verification of HDL Models”, Second Edition, Springer, 2003.

HARDWARE SOFTWARE CO-DESIGN (23MTVLE15)

(Elective V)

Course Category	**PE/ELECTIVE-V**	Credits	**3**
Course Type	**Theory**	L-T-P	**3-0-0**
Year	**II**	CIE Marks	**25**
Sem.	**I**	SEE Marks	**75**
		TOTAL MARKS	**100**

Course Outcomes

At the end ofc ourse, the student will be able to

Number	COURSE OUTCOMES (COs)	Blooms Taxonomy
CO1	About the Hardware-Software Codesign Methodology.	**L2**
CO2	How to select a target architecture and how a prototype is built and how emulation of a prototype is done.	**L3**
CO3	Briefviewaboutcompilationtechnologiesandcompilerdevelopmentenvironment.	**L4**
CO4	Understandtheimportanceofsystemlevelspecificationlanguagesandmulti-languageco-simulation.	**L2**

Note: *L1-Remember, L2–Understand, L3–Apply, L4–Analyze, L5 –Evaluate, L6 –Create*

COURSE CONTENTS

UNIT-I:

Co- Design Issues: Co-Design Models, Architectures, Languages, A Generic Co-design Methodology. **Co-Synthesis Algorithms:** Hardware software synthesis algorithms: hardware –software partitioning distributed system co-synthesis.

UNIT-II:

Prototyping and Emulation

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT-III:

Compilation Techniques and Tools for Embedded Processor Architectures

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT-IV:

Design Specification and Verification

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, Interface verification.

UNIT-V:

Languages for System-Level Specification and Design-I

System-level specification, design representation for system level synthesis, system level specification languages.

Languages for System-Level Specification and Design-II

Heterogeneous specifications and Multilanguage co-simulation, the cosymasystem and Lycossystem.

Text Books:

1. Hardware/Software Co-Design Principles and Practice –Jorgen Staunstrup, Wayne Wolf –2009, Springer.
2. Hardware/Software Co-Design-Giovanni DeMicheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers

Reference Books:

1. A Practical Introduction to Hardware/Software Co-design –Patrick R. Schaumont-2010–Springer Publications.

BUSINESS ANALYTICS (23MTVLOE1)
(Open Elective)

Course Category	**OE/ELECTIVE-1**	Credits	**3**
Course Type	**Theory**	L-T-P	**3-0-0**
Year	**II**	CIE Marks	**25**
Sem.	**I**	SEE Marks	**75**
		TOTAL MARKS	**100**

Course Outcomes

At the end of course, the student will be able to

Number	COURSEOUTCOMES(COs)	Blooms Taxonomy
CO1	Demonstrate knowledge of data analytics.	**L2**
CO2	Demonstrate the ability of think critically in making decisions based on data and deep analytics.	**L2**
CO3	Demonstrate the ability to use technical skills in predicative and prescriptive modelling to support business decision-making.	**L2**
CO4	Demonstrate the ability to translate data into clear, actionable insights	**L2**

Note: *L1-Remember, L2–Understand, L3–Apply, L4–Analyze, L5 –Evaluate, L6 –Create*

COURSE CONTENTS

UNIT1:

Business analytics: Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organization, competitive advantages of Business Analytics.

Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modelling, sampling and estimation methods overview.

UNIT 2:

Trendiness and Regression Analysis: Modelling Relationships and Trends in Data, simple Linear Regression. Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology

UNIT 3:

Organization Structures of Business analytics, Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, Measuring contribution of Business analytics, Managing Changes. Descriptive Analytics, predictive analytics, predicative Modelling, Predictive analytics analysis, Data Mining, Data Mining Methodologies, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modelling, nonlinear Optimization.

UNIT 4:

Forecasting Techniques: Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models.

Monte Carlo Simulation and Risk Analysis: Monte Carle Simulation Using Analytic Solver Platform, New-Product Development Model, Newsvendor Model, Overbooking Model, Cash Budget Model.

UNIT 5:

Decision Analysis: Formulating Decision Problems, Decision Strategies with the without Outcome Probabilities, Decision Trees, The Value of Information, Utility and Decision Making. Recent Trends in: Embedded and collaborative business intelligence, Visual data recovery, Data Storytelling and Data journalism

Reference:

1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson FT Press.
2. Business Analytics by James Evans, persons Education.

INDUSTRIAL SAFETY (23MTVLOE2)

(Open Elective)

Course Category	**OE/ELECTIVE-2**	Credits	**3**
Course Type	**Theory**	L-T-P	**3-0-0**
Year	**II**	CIE Marks	**25**
Sem.	**I**	SEE Marks	**75**
		TOTAL MARKS	**100**

COURSE CONTENTS

UNIT-1:

Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

UNIT-2:

Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

UNIT-3:

Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

UNIT-4:

Fault tracing: Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree

for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment's like, I. Anyone machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

UNIT-5:

Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

Reference:

1. Maintenance Engineering Handbook, Higgins & Morrow, DaInformation Services.
2. Maintenance Engineering, H.P. Garg, S. Chandand Company.
3. Pump-hydraulic Compressors, Audels, Mcgrew Hill Publication.
4. Foundation Engineering Handbook, Winterkorn, Hans, Chapman & Hall London

OPERATIONS RESEARCH (23MTVLOE3)

(Open Elective)

Course Category	**OE/ELECTIVE-3**	Credits	**3**
Course Type	**Theory**	L-T-P	**3-0-0**
Year	**II**	CIE Marks	**25**
Sem.	**I**	SEE Marks	**75**
		TOTAL MARKS	**100**

COURSE OUTCOMES

At the end of course, the student will be able to

Number	COURSEOUTCOMES(COs)	Blooms Taxonomy
CO1	Apply the dynamic programming to solve problems of discreet and continuous variables.	**L3**
CO2	Apply the concept of non-linear programming	**L3**
CO3	Carry out sensitivity analysis	**L4**
CO4	Model the real world problem and simulate it.	**L6**

Note: *L1-Remember, L2–Understand, L3–Apply, L4–Analyze, L5 –Evaluate, L6 –Create*

COURSE CONTENTS

UNIT 1

Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models

UNIT 2

Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametric programming

UNIT 3:

Nonlinear programming problem-Kuhn-Tucker conditions mincostflow problem-maxflow problem - CPM/PERT

UNIT 4

Scheduling and sequencing-single server and multiple server models-deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

UNIT 5

Competitive Models, Single and Multi-channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation

References:

1. H.A. Taha, Operations Research, An Introduction, PHI, 2008
2. H.M. Wagner, Principles of Operations Research, PHI, Delhi,1982.
3. J.C. Pant, Introduction to Optimization: Operations Research, Jain Brothers, Delhi, 2008
4. Hitler Libermann Operations Research: McGraw Hill Pub, 2009
5. Pannerselvam, Operations Research: Prentice Hall of India 2010
6. Harvey M Wagner, Principles of Operations Research: Prentice Hall of India 2010

COST MANAGEMENT OF ENGINEERING PROJECTS

(23MTVLOE4) (Open Elective)

Course Category	**OE/ELECTIVE-4**	Credits	**3**
Course Type	**Theory**	L-T-P	**3-0-0**
Year	**II**	CIE Marks	**25**
Sem.	**I**	SEE Marks	**75**
		TOTAL MARKS	**100**

COURSE CONTENTS

Introduction and Overview of the Strategic Cost Management Process

Cost concepts in decision-making; Relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision-Making.

Project: meaning, Different types, why to manage, cost overruns centres, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and non- technical activities. Detailed Engineering activities. Pre project execution main clearances and documents Project team: Role of each member. Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process

Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision- making problems. Standard costing and Variance Analysis. Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector. Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints. Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value- Chain Analysis. Budgetary Control; Flexible Budgets; Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing.

Quantitative techniques for cost management, Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Simulation, Learning Curve Theory.

References:

1. Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi
2. Charles T. Horngren and George Foster, Advanced Management Accounting
3. Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting
4. Ashish K.Bhattacharya, Principles & Practices of Cost Accounting A.H. Wheeler publisher
5. N.D. Vohra, Quantitative Techniques in Management, Tata McGraw Hill Book Co. Ltd.

COMPOSITE MATERIALS (23MTVLOE5)

(Open Elective)

Course Category	**OE/ELECTIVE-5**	Credits	**3**
Course Type	**Theory**	L-T-P	**3-0-0**
Year	**II**	CIE Marks	**25**
Sem.	**I**	SEE Marks	**75**
		TOTAL MARKS	**100**

COURSE CONTENTS

UNIT–I:

INTRODUCTION: Definition – Classification and characteristics of Composite materials. Advantages and application of composites. Functional requirements of reinforcement and matrix.Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.

UNIT– II:

REINFORCEMENTS: Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers. Properties and applications of whiskers, particle reinforcements. Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures. Isostrain and Isostress conditions.

UNIT– III:

Manufacturing of Metal Matrix Composites: Casting – Solid State diffusion technique, Cladding– Hot isostatic pressing. Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving. Properties and applications.

UNIT–IV:

Manufacturing of Polymer Matrix Composites: Preparation of Moulding compounds and prepregs – hand layup method – Autoclave method – Filament winding method – Compression moulding – Reaction injection moulding. Properties and applications.

UNIT– V:

Strength: Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

Text Books:

1. Material Science and Technology–Vol 13 – Composites by R.W. Cahn–VCH, West Germany.
2. Materials Science and Engineering, An introduction. WD Callister, Jr., Adapted by R. Balasubrahmaniam, John Wiley & Sons, NY, Indian edition,2007.

References:

1. Hand Book of Composite Materials-ed-Lubin.
2. Composite Materials–K.K.Chawla.
3. Composite Materials Science and Applications – Deborah D.L. Chung.

WASTE TO ENERGY (23MTVLOE6)

(Open Elective)

Course Category	**OE/ELECTIVE-6**	Credits	**3**
Course Type	**Theory**	L-T-P	**3-0-0**
Year	**II**	CIE Marks	**25**
Sem.	**I**	SEE Marks	**75**
		TOTAL MARKS	**100**

COURSE CONTENTS

UNIT -I:

Introduction to Energy from Waste: Classification of waste as fuel – Agro based, Forest residue, Industrial waste-MSW–Conversion devices–Incinerators, gasifiers, digestors

UNIT-II:

Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

UNIT-III:

Biomass Gasification: Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement forthermalheating–Gasifierenginearrangementandelectricalpower–Equilibriumandkinetic consideration in gasifier operation

UNIT-IV:

Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

UNIT-V:

Biogas: Properties of biogas (Calorific value and composition)-Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct

combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

References:

1. Non Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 1990.
2. Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., Vol. I & II, Tata McGraw Hill Publishing Co. Ltd., 1983.
3. Food, Feed and Fuel from Biomass, Challal, D.S., IBH Publishing Co. Pvt. Ltd., 1991.
4. Biomass Conversion and Technology, C.Y. Were Ko-Brobby and E.B. Hagan, John Wiley & Sons, 1996.

DISSERTATION PHASE -I /INDUSTRIAL PROJECT

(to be continued and evaluated next semester)

(23MTVLP02)

Course Category	**PROJECT**	Credits	**10**
Course Type	**PRACTICAL**	L-T-P	**0-0-10**
Year	**II**	Sem.	**I**

Syllabus Contents:

The dissertation / project topic should be selected / chosen to ensure the satisfaction of the urgent need to establish a direct link between education, national development and productivity and thus reducet he gap between the world of work and the world of study. The dissertation should have the following

- Relevance to social needs of society
- Relevance to value addition to existing facilities in the institute
- Relevance to industry need
- Problems of national importance
- Research and development in various domain

The student should complete the following:

- Literature survey Problem Definition
- Motivation for study and Objectives
- Preliminary design / feasibility/ modular approaches
- Implementation and Verification
- Report and presentation

The dissertation stage II is based on are port prepared by the students on dissertation allotted to them. It may be based on:

- Experimental verification /Proof of concept.
- Design, fabrication, testing of Communication System.
- The viva-voce examination will be based on the above report and work.

Guidelines for Dissertation Phase –I and II at M.Tech. (Electronics):

- As per the AICTE directives, the dissertation is a yearlong activity, to be carried out and evaluated in two phases i.e. Phase – I: July to December and Phase – II: January to June.
- The dissertation may be carried out preferably in-house i.e. department's laboratories and centers OR in industry allotted through department's T & P coordinator.
- After multiple interactions with guide and based on comprehensive literature survey, the student shall identify the domain and define dissertation objectives. The referred literature should preferably include IEEE/IET/IETE/Springer/Science Direct/ACM journals in the areas of Computing and Processing (Hardware and Software), Circuits-Devices and Systems, Communication-Networking and Security, Robotics and Control Systems, Signal Processing and Analysis and any other related domain. In case of Industry sponsored projects, the relevant application notes, while papers, product catalogues should be referred and reported.
- Student is expected to detail out specifications, methodology, resources required, critical issues involved in design and implementation and phase wise work distribution, and submit the proposal within a month from the date of registration.
- Phase – I deliverables: A document report comprising of summary of literature survey, detailed objectives, project specifications, paper and/or computer aided design, proof of concept/functionality, part results, A record of continuous progress.
- Phase – I evaluation: A committee comprising of guides of respective specialization shall assess the progress/performance of the student based on report, presentation and Q&A. In case of unsatisfactory performance, committee may recommend repeating the Phase-I work.
- During phase – II, student is expected to exert on design, development and testing of the proposed work as per the schedule. Accomplished results/contributions/innovations should be published in terms of research papers in reputed journals and reviewed focused conferences OR IP/Patents.
- Phase – II deliverables: A dissertation report as per the specified format, developed system in the form of hardware and/or software, a record of continuous progress.
- Phase – II evaluation: Guide along with appointed external examiner shall assess the progress/performance of the student based on report, presentation and Q&A. In case of unsatisfactory performance, committee may recommend for extension or repeating the work

AUDIT 1 and 2: ENGLISH FOR RESEARCH PAPER WRITING (23MTVLAD1)

Course objectives:

Students will be able to:

- Understandthathowtoimproveyourwritingskillsandlevelofreadability Learn about what to write in each section
- Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission

Syllabus

Units	CONTENTS	Hours
1	Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness	4
2	Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction	4
3	Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.	4
4	Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature,	4
5	Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions	4
6	Useful phrases, how to ensure paper is as good as it could possibly be the first-time submission	4

Suggested Studies:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book.
4. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

AUDIT 1 and 2: DISASTER MANAGEMENT (23MTVLAD2)

Course Objectives:- Students will be able to:

- Learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- Critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they workin

Syllabus

Units	CONTENTS	Hours
1	**Introduction** Disaster: Definition, Factors And Significance; Difference Between Hazard And Disaster; Natural And Manmade Disasters: Difference, Nature, Types And Magnitude.	4
2	**Repercussions of Disasters and Hazards**: Economic Damage, Loss Of Human And Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man- made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.	4
3	**Disaster Prone Areas in India** Study Of Seismic Zones; Areas Prone To Floods And Droughts, Landslides And Avalanches; Areas Prone To Cyclonic And Coastal Hazards With Special Reference To Tsunami; Post-Disaster Diseases And Epidemics	4
4	**Disaster Preparedness and Management** Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application Of Remote Sensing, Data From Meteorological And Other Agencies, Media Reports: Governmental And Community Preparedness.	4
5	**Risk Assessment** Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation In Risk Assessment And Warning, People's Participation In Risk Assessment. Strategies for Survival.	4

6	**Disaster Mitigation** Meaning, Concept And Strategies Of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation And Non-Structural Mitigation, Programs Of Disaster Mitigation In India.	4

Suggested Readings:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies" New Royal Book Company.
2. Sahni, Pardeep Et. Al. (Eds.), "Disaster Mitigation Experiences and Reflections", Prentice Hall Of India, New Delhi.
3. Goel S. L., Disaster Administration and Management Text And Case Studies", Deep & Deep Publication Pvt. Ltd., New Delhi.

AUDIT 1 and 2: SANSKRIT FOR TECHNICAL KNOWLEDGE (23MTVLAD3)

Course Objectives

- To get a working knowledge in illustrious Sanskrit, the scientific language in the world
- Learning of Sanskrit to improve brain functioning
- Learning of Sanskrit to develop the logic in mathematics, science & other subjects enhancing the memory power
- The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature.

Syllabus

Unit	Content	Hours
1	Alphabets in Sanskrit, Past/Present/Future Tense, Simple Sentences	8
2	Order Introduction of roots Technical information about Sanskrit Literature	8
3	Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics	8

Suggested reading

1. "Abhyas pustakam" – Dr. Vishwas, Samskrita-Bharti Publication, New Delhi
2. "Teach Yourself Sanskrit" Prathama Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication
3. "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi.

Course Output

Students will be able to

1. Understanding basic Sanskrit language
2. Ancient Sanskrit literature about science & technology can be understood
3. Being a logical language will help to develop logic in students

AUDIT 1 and 2: VALUE EDUCATION (23MTVLAD4)

Course Objectives

Students will be able to

- Understand value of education and self-development
- Imbibe good values in students
- Let the should know about the importance of character

Syllabus

Unit	Content	Hours
1	• Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. • Moral and non-moral valuation. Standards and principles. • Value judgments	4
2	• Importance of cultivation of values. • Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. • Honesty, Humanity. Power of faith, National Unity. • Patriotism. Love for nature, Discipline	6
3	• Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline. • Punctuality, Love and Kindness. • Avoid fault Thinking. • Free from anger, Dignity of labour. • Universal brother hood and religious tolerance. • True friendship. • Happiness Vssuffering, love for truth. • Aware of self-destructive habits. • Association and Cooperation. • Doing best for saving nature	6

4	) Character and Competence –Holy books vs Blind faith.) Self-management and Good health.) Science of reincarnation.) Equality, Nonviolence, Humility, Role of Women.) All religions and same message.) Mind your Mind, Self-control.) Honesty ,Studying effectively	6

Suggested reading

1. Chakroborty, S.K. "Values and Ethics for organizations Theory and practice", Oxford University Press, New Delhi

Course outcomes

Students will be able to

1. Knowledge of self-developmentS
2. Learn the importance of Human values
3. Developing the overall personality

AUDIT 1 and 2: CONSTITUTION OF INDIA (23MTVLAD5)

Course Objectives:

Students will be able to:

- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals "constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement o f the Bolshevik Revolution in1917anditsimpacton the initial drafting of the Indian Constitution.

Syllabus

Units	Content	Hours
1	**History of Making of the Indian Constitution:** History Drafting Committee, (Composition & Working)	4
2	**Philosophy of the Indian Constitution:** Preamble Salient Features	4
3	**Contours of Constitutional Rights & Duties:** Fundamental Rights Right to Equality Right to Freedom Right against Exploitation Right to Freedom of Religion Cultural and Educational Rights Right to Constitutional Remedies Directive Principles of State Policy Fundamental Duties.	4
4	**Organs of Governance:** Parliament Composition Qualifications and Disqualifications Powers and Functions Executive President Governor Council of Ministers Judiciary, Appointment and Transfer of Judges, Qualifications Powers and Functions	4

5	**Local Administration:** District"s Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CE of Municipal Corporation. Pachayatiraj: Introduction, PRI: ZilaPachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy	4
6	**Election Commission:** Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.	4

Suggested reading

1. The Constitution of India, 1950 (BareAct), Government Publication.
2. Dr. S.N. Busi, Dr. B.R. Ambedkar framing of Indian Constitution,1st Edition, 2015.
3. M.P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

Course Outcomes:

Students will be able to:

1. Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
2. Discuss the intellectual origins of the frame work of argument that informed the conceptualization of social reforms leading to revolution in India.
3. Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
4. Discuss the passage of the Hindu Code Bill of 1956.

AUDIT 1 and 2: PEDAGOGY STUDIES (23MTVLAD6)

Course Objectives:

Students will be able to:

1. Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.
2. Identify critical evidence gaps to guide the development.

Syllabus

Units	Content	Hours
1	**Introduction and Methodology:** J Aims and rationale, Policy background, Conceptual framework and terminology J Theories of learning, Curriculum, Teacher education. J Conceptual frame work, Research questions. J Overview of methodology and Searching.	4
2	J The matic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. J Curriculum, Teacher education.	2
3	J Evidence on the effectiveness of pedagogical practices J Methodology for the in depth stage: quality assessment of included studies. J How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? J Theory of change. J Strength and nature of the body of evidence for effective pedagogical practices. J Pedagogic theory and pedagogical approaches. J Teacher's attitudes and beliefs and Pedagogic strategies.	4
4	J Professional development: alignment with class room practices and follow-up support J Peer support J Support from the head teacher and the community. J Curriculum and assessment J Barriers to learning: limited resources and large class sizes	4
5	**Research gaps and future directions** J Research design J Contexts J Pedagogy J Teacher education J Curriculum and assessment J Dissemination and research impact.	2

Suggested reading

1. AckersJ, HardmanF(2001)ClassroominteractioninKenyanprimaryschools,Compare,31 (2):245-261.
2. Agrawal M (2004) Curricularre for min schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.
4. Akyeampong K, Lussier K, Pryor J, West brook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: Amassscale, rapid, learning to read‟ campaign. www.pratham.org/images/resource%20working%20paper%202.pdf.

Course Outcomes:

Students will be able to understand:

1. What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
2. What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
3. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

AUDIT 1 and 2: STRESS MANAGEMENT BY YOGA

(23MTVLAD7)

Course Objectives

1. To achieve overall health of body and mind
2. To overcome stress

Syllabus

Unit	Content	Hours
1	) Definitions of Eight parts of yog. (Ashtanga)	8
2	Yamand Niyam. Do`s and Don'ts in life. i) Ahinsa, satya, astheya, bramhacharya and a parigraha ii) Shaucha, santosh,tapa,swadhyay,ishwarpranidhan	8
3	) Asan and Pranayam 1. Various yog poses and their benef its for mind & body 2. Regularization of breathing techniques and its effects-Types of pranayam	8

Suggested reading

1. "Yogic Asanas for Group Tarining - Part-I": Janardan Swami Yogabhyasi Mandal, Nagpur
2. "Rajayoga or conquering the Internal Nature" bySwami Vivekananda, Advaita Ashrama (Publication Department), Kolkata

Course Outcomes:

Students will be able to:

1. Develop healthy mind in a healthy body thus improving social health also
2. Improve efficiency

AUDIT 1 and 2: PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS (23MTVLAD8)

Course Objectives

1. To learn to achieve the highest goal happily
2. To become a person with stable mind, pleasing personality and determination.
3. To awaken wisdom in students

Syllabus

Unit	Content	Hours
1	Neeti satakam – Holistic development of personality ⟩ Verses-19,20,21,22 (wisdom) ⟩ Verses-29,31,32 (pride & heroism) ⟩ Verses-26,28,63,65 (virtue) ⟩ Verses-52,53,59 (don't's) ⟩ Verses-71,73,75,78 (do's)	8
2	⟩ Approach to day to day work and duties. ⟩ Shrimad Bhagwad Geeta: Chapter 2 – Verses 41, 47, 48, ⟩ Chapter 3 – Verses 13, 21, 27, 35, Chapter 6 –Verses 5, 13, 17, 23, 35, ⟩ Chapter 18 - Verses 45, 46, 48.	8
3	⟩ Statements of basic knowledge. ⟩ Shrimad Bhagwad Geeta: Chapter 2 – Verses 56, 62, 68 ⟩ Chapter12 -Verses 13,14, 15, 16,17, 18 ⟩ Personality of Role model. Shrimad Bhagwad Geeta: Chapter 2 - Verses 17, Chapter 3 - Verses 36, 37, 42, ⟩ Chapter 4 - Verses18, 38, 39 ⟩ Chapter 18 – Verses 37, 38, 63	8

Suggested reading

1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P. Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.

Course Outcomes

Students will be able to

1. Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life
2. The person who has studied Geeta will lead the nation and mankind to peace and prosperity
3. Study of Neetishatakam will help in developing versatile personality of students